The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A process of forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy, the process comprising:

forming a diffusion barrier layer on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer over the diffusion barrier layer, the diffusion barrier layer located between the first conductive layer and the under bump metallurgy; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the diffusion barrier layer, wherein the second conductive layer has a different composition than the first conductive layer.

2. The process of Claim 1 wherein the diffusion barrier layer comprises copper or nickel.

3. The process of Claim 1, wherein the first conductive layer comprises tin, silver, copper, gold, or bismuth.

4. The process of Claim 3, wherein the first conductive layer comprises tin or silver.

5. The process of Claim 1, wherein the second conductive layer comprises tin, silver, copper, gold, or bismuth.

6. The process of Claim 5, wherein the second conductive layer comprises tin or silver.

7. The method of Claim 1 further comprising forming at least one additional conductive layer over the diffusion barrier layer.

8. The method of Claim 7, wherein the at least one additional conductive layer comprises tin, silver, copper, gold, or bismuth.

9. The method of Claim 1, wherein the diffusion barrier layer is formed by electrolytic deposition.

10. The method of Claim 1, wherein either the first or the second conductive layer is free of tin and silver.

11. A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming a lead-free first conductive layer on a surface of the microelectronic workpiece;

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer; and

forming a lead-free third conductive layer over the second conductive layer, the second conductive layer located between the third conductive layer and the first conductive layer, wherein the third conductive layer has a different composition than the second conductive layer.

12. The method of Claim 11, wherein the first, second, and third conductive layers comprise tin, silver, copper, gold, or bismuth.

13. The method of Claim 11, wherein the first, second, and third conductive layers comprise tin, silver, or copper.

14. The process of Claim 11, further comprising the step of forming at least one additional conductive layer.

15. The process of Claim 14, wherein the at least one additional conductive layer comprises tin, silver, copper, gold, or bismuth.

16. A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming a lead-free first conductive layer on a surface of the microelectronic workpiece; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer, at least one of the first and second conductive layers comprising an alloy of at least two conductive materials.

17. The process of Claim 16, wherein the first and second conductive layers comprise tin, silver, copper, gold, or bismuth.

18. The method of Claim 16, wherein the at least two conductive materials are selected from tin, silver, copper, gold, and bismuth.

19. The method of Claim 16, further comprising forming at least one additional conductive layer over the surface of the microelectronic workpiece.

20. The method of Claim 19, wherein the additional conductive layer comprises tin, silver, copper, gold, or bismuth.

21. A process of forming a solder alloy precursor on a microelectronic workpiece comprising:

forming a lead-free first conductive layer on a surface of the microelectronic workpiece; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the surface of the microelectronic workpiece, wherein the second conductive layer has a different composition than the first conductive layer, wherein the second conductive layer is formed by substitutional reduction.

22. The method of Claim 21, wherein the first and second conductive layers comprise tin, silver, copper, gold, or bismuth.

23. The method of Claim 21, wherein the first and second conductive layers comprise tin or silver.

24. The method of Claim 21 further comprising the step of forming at least one additional conductive layer over the microelectronic workpiece.

25. The process of Claim 24, wherein the at least one additional conductive layer comprises tin, silver, copper, gold, or bismuth.

26. The method of Claim 21, wherein the second layer comprises silver, copper, gold, or bismuth.

27. A tool for forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy, said tool comprising one or more stations for:

forming a diffusion barrier layer on the exposed portions of the conductive under bump metallurgy;

forming a lead-free first conductive layer over the diffusion barrier layer, the diffusion barrier layer located between the first conductive layer and the under bump metallurgy; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the diffusion barrier layer, the second conductive layer having a different composition than the first conductive layer.

28. The tool of Claim 27, wherein the station for forming a diffusion barrier layer comprises a reactor for electrolytically depositing the diffusion barrier layer.

29. The tool of Claim 27 further comprising a source of copper or nickel.

30. The tool of Claim 27, wherein the station for forming the first conductive layer comprises a reactor for electrolytically depositing the first conductive layer.

31. The tool of Claim 30 further comprising a source of tin, silver, copper, gold, or bismuth.

32. The tool of Claim 27, wherein the station for forming the second conductive layer comprises a reactor for electrolytically depositing the second conductive layer.

33. The tool of Claim 32 further comprising a source of tin, silver, copper, gold, or bismuth.

34. The tool of Claim 27, further comprising a station for rinsing the workpiece.

35. The tool of Claim 27, further comprising a station for pre-wetting the workpiece.

36. A tool for forming a solder alloy precursor on the surface of a microelectronic workpiece, including conductive under bump metallurgy, said tool comprising one or more stations for:

forming a lead-free first conductive layer over the conductive under bump metallurgy;

depositing a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the conductive under bump metallurgy, wherein the second conductive layer has a different composition than the first conductive layer; and

forming a lead-free third conductive layer over the second conductive layer, the second conductive layer located between the third conductive layer and the first conductive layer, wherein the third conductive layer has a different composition than the second conductive layer.

37. A tool for forming a solder alloy precursor on a microelectronic workpiece including conductive under bump metallurgy, said tool comprising one or more stations for:

forming a lead-free first conductive layer over the conductive under bump metallurgy; and

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the conductive under bump metallurgy, wherein the second conductive layer has a different composition than the first conductive layer, at least one of the conductive layers being an alloy comprising at least two conductive materials.

38. The tool of Claim 37, wherein either the station for forming the first conductive layer or the station for forming the second conductive layer includes a source of at least two metals selected from tin, silver, copper, gold, or bismuth.

39. A tool for forming a solder alloy precursor on the surface of a microelectronic workpiece including conductive under bump metallurgy, said tool comprising one or more stations for:

forming a lead-free first conductive layer over the conductive under bump metallurgy;

forming a lead-free second conductive layer over the first conductive layer, the first conductive layer located between the second conductive layer and the conductive under bump metallurgy, wherein the second conductive layer has a different composition than the first conductive layer and is formed by substitutional reduction.

40. A tool for forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy, the tool comprising:

a diffusion barrier layer deposition reactor including a source of copper or nickel,

a first conductive layer deposition reactor including a source of a first conductive material;

a second conductive layer deposition reactor including a source of a second conductive material different from the first conductive material.

41. A tool for forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy, the tool comprising:

a first conductive layer deposition reactor including a source of a first conductive material;

a second conductive layer deposition reactor including a source of a second conductive material different from the first conductive material;

a third conductive layer deposition reactor including a source of a third conductive material different from the second conductive material.